Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SOURCE**

**GATE**

**.019”**

**.102”**

**Top Material: Al**

**Backside Material: Cr Ni Ag**

**Bond Pad Size: G = .018” X .023” S = .023” X .033”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .091” X .102” DATE: 4/27/23**

**MFG: INT’L RECTIFIER THICKNESS .016” P/N: IRFC220**

**DG 10.1.2**

#### Rev B, 7/19/02